Physical Layer Interface Implementation Agreement

FRF.14

Frame Relay Forum Technical Committee
December 1998

Note: The user's attention is called to the possibility that implementation of the frame relay implementation agreement contained herein may require the use of inventions covered by patent rights held by third parties. By publication of this frame relay implementation agreement the Frame Relay Forum makes no representation that the implementation of the specification will not infringe on any third party rights. The Frame Relay Forum take no position with respect to any claim that has been or may be asserted by any third party, the validity of any patent rights related to any such claims, or the extent to which a license to use any such rights may not be available.

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Revision History

Version	Change	Date
FRF.14	Initial Version	December 14, 1998

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1 Introduction

1.1 Purpose

Frame Relay standards defined in [1] and [2] specify frame formats and procedures for the transfer of data using frame relaying networks. These standards do not address the characteristics of the physical interface at a UNI or NNI. Frame relay operates successfully over a diverse set of physical interfaces that are defined by a variety of standards organizations including the International Telecommunication Union (ITU) and national standards bodies (e.g., the American National Standards Institute (ANSI)).

This implementation agreement enhances interoperability between frame relay devices by identifying common, recommended physical interface types and their critical characteristics. This implementation agreement does not mandate or prohibit any specific physical interface. Further, this agreement is not intended as the basis for frame relay conformance testing.

To ensure the best interoperability between frame relay devices, implementation of at least one of the interfaces described in this document is highly recommended. If an implementation claims compliance with this agreement for an interface addressed by the agreement, the implementation of the interface should follow the guidelines of this document.

Some of the material contained in this agreement has been drawn from other Frame Relay Forum Implementation Agreements. This agreement does not make obsolete implementations compliant with the following Frame Relay Forum Implementation Agreements:

- Section 1.1 of FRF 1.1;
- Section 2.1 of FRF 2.1;
- Section 4 of FRF 4; and
- Section 10 of FRF 10.

Future changes to these Implementation Agreements will reference this Implementation Agreement for specification of physical interface characteristics. New interface Implementation Agreements developed by the Frame Relay Forum will reference this agreement.

1.2 Definitions

Must, **Shall**, or **Mandatory** — the item is an absolute requirement of the implementation agreement.

Should — the item is highly desirable.

May or **Optional** — the item is not compulsory, and may be followed or ignored according to the needs of the implementor.

1.3 Acronym List

ANSI	American National Standards Institute
ATM	Asynchronous Transfer Mode
CCC	Clear Channel Capability
CSU	Channel Service Unit

DCE	Data Circuit-terminating Equipment
DS1	Digital Signal Level 1
DS3	Digital Signal Level 3
DSU	Data Service Unit
DTE	Data Terminal Equipment
E3	G.703 34.368 Mbps Interface
FDDI	Fiber Distributed Data Interface
HDLC	High-level Data Link Control
HSSI	High Speed Serial Interface
ISDN	Integrated Services Digital Network
ISO	International Standards Organization
ITU	International Telecommunication Union
kbit/s	Kilobits per second
Kbps	Kilobits per second
Mbit/s	Megabits per second
Mbps	Megabits per second
NNI	Network-to-Network Interface
SDH	Synchronous Digital Hierarchy
SONET	Synchronous Optical Network
SPE	Synchronous Payload Envelope
STM	Synchronous Transfer Mode
STS	Synchronous Transport Signal
UNI	User-to-Network Interface
VT	Virtual Tributary

1.4 Relevant Standards

The following is a list of standards on which these implementation agreements are based:

[1] ITU Recommendation Q.922, ISDN Data Link Layer Specification for Frame Mode Bearer Services, ITU, Geneva, 1992.

[2] ITU Recommendation Q.933, ISDN Signaling Specification for Frame Mode Bearer Services, ITU, Geneva, 1995.

[3] ANSI/EIA/TIA-530-A-1992, High Speed 25-Position Interface for Data Terminal Equipment and Data Circuit-Terminating Equipment, Including Alternative 26-Position Connector, American National Standards Institute, New York, 1992.

[4] ITU Recommendation V.24, List of Definitions For Interchange Circuits Between Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE), ITU, Geneva, 1993.

[5] EIA-422-A, Electrical Characteristics of Balanced Voltage Digital Interface Circuits.

[6] ISO 2110:1989/Amd. 1:1991, 25-Pole DTE/DCE Interface Connector and Contact Number Assignments.

[7] ANSI T1.107-1995, Digital hierarchy – Formats specifications , American National Standards Institute, New York, 1995.

[8] ANSI T1.403, Carrier to Customer Installation DS1 Metallic Interface, American National Standards Institute, New York, 1995.

[9] ANSI/TIA/EIA-612-1993, Electrical Characteristics for an Interface at Data Signaling Rates up to 52 Mbit/s, American National Standards Institute, New York, 1993.

[10] ANSI/TIA/EIA/-613-1993, High Speed Serial Interface for Data Terminal Equipment and Data Circuit-Terminating Equipment, American National Standards Institute, New York, 1993.

[11] ITU Recommendation G.703, Physical/electrical characteristics of hierarchical digital interfaces, ITU, Geneva, 1988.

[12] ITU Recommendation G.704, Synchronous Frame Structures used at Primary and Secondary Hierarchical Levels ITU, Geneva, 1991.

[13] IETF RFC 1662, PPP in HDLC-like Framing, W. Simpson (ed.), July 1994.

[14] ISO/IEC 2593 – 1993, Information technology - Telecommunications and information exchange between systems - 34 pole DTE/DCE interface connector mateability dimensions and contact number assignments.

[15] ISO/IEC 4902 – 1989, Information technology - Data communication - 37 pole DTE/DCE interface connector and contact number assignments.

[16] ISO/IEC 4903 – 1989, Information technology - Data communication - 15 pole DTE/DCE interface connector and contact number assignments.

[17] ITU Recommendation V.11, Electrical characteristics for balanced double-current interchange circuits operating at data signalling rates up to 10 Mbit/s, ITU, Geneva, 1993.

[18] ITU Recommendation V.24, List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE), ITU, Geneva, 1993.

[19] ITU Recommendation V.28, Electrical characteristics for unbalanced double-current interchange circuits, ITU, Geneva, 1993.

[20] ITU Recommendation V.35, Data transmission at 48 kilobits per second using 60-108 kHz Group Band Circuits, ITU, Geneva, 1988.

[21] ITU Recommendation V.36, Modems for synchronous data transmission using 60-108 kHz group band circuits, ITU, Geneva, 1988.

[22] ITU Recommendation V.37, Synchronous data transmission at a data signalling rate higher than 72 kbit/s using 60-108 kHz group band circuits, ITU, Geneva, 1988.

[23] ITU Recommendation X.21, Interface between data terminal equipment and data circuit-terminating equipment for synchronous operation on public data networks, ITU, Geneva, 1992.

[24] ITU Recommendation X.27, Electrical characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications, ITU, Geneva, 1993.

[25] ITU Recommendation Q.921, ISDN User-Network Interface-Data Link Layer Specification, ITU, Geneva, 1993.

[26] ITU Recommendation G.832, Transport of SDH elements on PDH networks: Frame and multiplexing structures, ITU, Geneva, 1995.

[27] ITU Recommendation G.751, Digital multiplex equipment operating at the third order bit rate of 34 368 kbit/s and the fourth order bit rate of 139 264 kbit/s and using positive justification, ITU, Geneva, 1988.

[28] ANSI T1.404-1994, Network-to-Customer Installation - DS3 Metallic Interface Specification, American National Standards Institute, New York, 1994.

[29] ANSI T1.404a-1996, Network-to-Customer Installation - DS3 Metallic Interface Specification Supplement, American National Standards Institute, New York, 1996.

[30] ANSI T1.105, Synchronous Optical Network (SONET) Basic Description including Multiplex Structure, Rates, and Formats, American National Standards Institute, New York, 1995.

[31] ITU Recommendation G.707, Network node interface for the synchronous digital hierarchy (SDH), ITU, Geneva, 1996.

[32] RFC 1619, W. Simpson (ed.), PPP over SONET/SDH, May 1994.

[33] ANSI T1.410-1992, Carrier-to-Customer Metallic Interface – Digital Data at 64 Kbit/s and Subrates, American National Standards Institute, New York, 1992.

[34] ITU-T Temporary Document 68rev.(PLEN) STUDY GROUP 15 Geneva, 9-20 February 1998 Questions: 9-14/15 SOURCE: WP3/15 TITLE: Report of WP3/15, Part I.

2 V.35 (ITU Recommendation V.35)

The V.35 interface [20] specifications are as follows:

1) Electrical characteristics according to ITU Recommendations V.35[20] and V.28 [19];

2) Connector and pin assignment according to ISO 2593 [14] and;

3) Interchange circuit definitions according to ITU Recommendation V.24 [18].

3 V.36/V.37 (ITU Recommendations V.36/V.37)

ITU recommendations V.36 [21] and V.37[22] specify the same connector (ISO 4902[15]), pin assignments, electrical characteristics, and interchange circuit functions. Therefore, only the V.37 text is referenced below. Applicable sections of V.37 are listed in the following sections.

3.1 Section 13.1, List of interchange circuits:

Support of the following balanced interchange circuits is required. Note 4 is ignored.

1) 103 Transmitted data

2) 104 Received data

3) 113 Transmitter signal element timing (DTE source)

4) 114 Transmitter signal element timing (DCE source)

5) 115 Receiver signal element timing (DCE source)

3.2 Section 13.2, Electrical Characteristics:

The following text applies: Use of electrical characteristics conforming to Recommendation V.11 [17] is required.

3.3 Section 13.2, Connector:

Section 13.2 specifies the 37-pin-D ISO 4902[15] connector. ISO 2110 amendment 1, 1991[6], specifies the 25-pin-D connector and the mapping of V.36/V.37 ISO 4902 pins to ISO 2110 pins. The mapping of pins is shown in Table B.1 of ISO 2110 amendment 1 (page 2). The 37-pin-D connector shall not be used. The following summarizes the pin assignments of the V.36/V.37 interface using the required 25-pin-D connector:

1) 103a - pin 2, 103b - pin 14
2) 104a - pin 3, 104b - pin 16
3) 113a - pin 24, 113b - pin 11
4) 114a - pin 15, 114b - pin 12
5) 115a - pin 17, 115b - pin 9

4 EIA-530 (ANSI/EIA/TIA-530)

The ANSI/EIA/TIA-530-A-1992 standard [3] specifies the electrical characteristics, connector and interchange circuits suitable for operation at all data rates below 2.1 Mpbs and is intended for use in all applications requiring a balanced electrical interface. This standard is in alignment with ITU Recommendation V.24 [18] and ISO 2110:1989/Amd. 1:1991 [6]. Applicable sections of ANSI/EIA/TIA-530- A-1992 are described in the following sections.

4.1 Electrical Characteristics

1) Section 2.1, Electrical Characteristics: The electrical characteristics of the specified balanced interchange circuits shall comply with EIA-422-A [5].
2) Section 2.1.1, Category I Circuits: This section identifies the Category I interchange circuits and stipulates that use of EIA-422-A balanced electrical characteristics for Category I circuits. The requirements of this section and Figure 2.1(a) shall apply. Category I interchange circuits CA, CB, CF and CJ are not applicable.

4.2 Required Balanced Interchange Circuits

1) The following Category I interchange circuits shall be supported:
    a) Circuit BA -- Transmitted Data
    b) Circuit BB -- Received Data
    c) Circuit DA -- Transmit Signal Element Timing, DTE Source
    d) Circuit DB -- Transmit Signal Element Timing, DCE Source
    e) Circuit DD -- Receiver Signal Element Timing, DCE Source
2) Section 2.3 Shield: The requirements of Section 2.3 shall be met.

3) Section 2.4 Circuit Grounding (Signal Common): The requirements of Section 2.4 and Figure 2.2 shall be met.

4.3 Connector and Pin Assignments

1) Section 3.1 Definition of Mechanical Interface: The requirements of Section 3.1 and Figure 3.1(a), shall apply. The alternative 26-position connector (Alt A) is not applicable.

2) Section 3.2 25-Position Interface Connector. The requirements of Section 3.2, including Figures 3.2, 3.3, 3.4, 3.5 and 3.6, shall apply.

3) Section 3.4 Connector Contact Assignments. The requirements of Section 3.4 shall apply. Applicable connector contact assignments from Figure 3.9 shall be implemented as shown in Table 1.

Circuit Mnemonic	ITU Number	Contact Number	Interchange Points	Circuit Name
		1		Shield
AB	102A	7	C-C'	Signal Common
AC	102B	23	C-C'	Signal Common
BA	103	2	A-A'	Transmitted Data
		14	B-B'	
BB	104	3	A-A'	Received Data
		16	B-B'	
DA	113	11	B-B'	Transmit Signal Element Timing DTE Source
		24	A-A'	
DB	114	12	B-B'	Transmit Signal Element Timing DCE Source
		15	A-A'	
DD	115	9	B-B'	Receiver Signal Element Timing DTE Source
		17	A-A'	

Table 1
Connector Contact Assignments For ANSI-530-A-1992

5 X.21 (ITU Recommendation X.21)

This unstructured interface uses the leased line (i.e., point to point) subset of the X.21 Recommendation [23]. The interface specifications are as follows:

1) Electrical characteristics according to ITU Recommendation X.27 (V.11) [24];

2) Connector and pin assignment according to ISO 4903 [16], and;

3) Interchange circuit definitions according to ITU Recommendation X.24 [18].

6 HSSI (ANSI/EIA/TIA-613)

The standard ANSI/TIA/EIA-613-1993 [10] together with ANSI/TIA/EIA-612-1993 [9] provides for a general purpose DTE-DCE interface for data rates up to a maximum of 53 Mbps employing bit-serial data over balanced interchange circuits.

6.1 Electrical Characteristics

Section 3 of ANSI/TIA/EIA-613, Signal Characteristics (which references ANSI/TIA/EIA-612) shall apply.

6.2 Required Interchange Circuits

Section 5 of ANSI/TIA/EIA-613, Functional Description of Interchange Circuits, shall apply with the exception of the interchange circuits and subsections listed in Table 2.

Circuit Number	Contact Pair	Circuit Name	Associated Section
107	3 & 28	DCE Ready	5.3.4
108/2	8 & 33	DTE Ready	5.3.5
143	10 & 35	Loopback A	5.3.6
144	12 & 37	Loopback B	5.3.6
142	24 & 49	Test Mode	5.3.7

Table 2
Interchange Circuit Exceptions for ANSI/TIA/EIA-613

6.3 Connector and Pin Assignments

1) Section 4.1 of ANSI/TIA/EIA-613, 50-Position Interface Connector, in its entirety, shall apply.

2) Section 4.2 of ANSI/TIA/EIA-613, Connector Contact Assignments, shall apply, with the following exceptions:

   a) 107 does not apply

   b) 108 / 2 does not apply

   c) 143 does not apply

   d) 144 does not apply

   e) 142 does not apply

7 56/64kbps (ANSI T1.410)

ANSI T1.410 [33] will be followed, with the following exceptions:

1) Multipoint and Secondary Channel services are not supported.

2) 2400, 4800, 9600, and 19200 rates are not supported.

3) Section 9.3 (Coding Restrictions) does not apply. This section is replaced by the following:

   In rare situations Frame Relay equipment operating at 64 kbit/s and supporting DSU latching loopback may be subject to inadvertent DSU latching due to the reception of a complex sequence of octets that is defined in section 10.3.2.2 of [33]. The ultimate source of this data may be Frame Relay equipment that is not operating at 64 kbit/s and is not subject to any payload pattern restrictions. Equipment typically deployed in existing networks for transmitting a Frame Relay payload at 64 kbit/s does not routinely take action to prevent inadvertent (re)transmission of this sequence. A Frame Relay-aware DSU may avoid inadvertent DSU latching loopback through the use of mechanisms that confirm that the received loopback pattern is an intended loopback code rather than a pseudo-random sequence of bytes that happen to make up a loopback code. These mechanisms may utilize timeouts or other heuristic approaches to prevent inadvertent DSU latching. While such mechanisms cannot guarantee that inadvertent loopback will never happen, they can reduce the likelihood of an occurrence.

4) Section 10.4 (64-kbit/s Synchronous Digital Data) is replaced by the following:

When operating at 64 kbit/s, Frame Relay customer equipment shall:

- Respond to CSU loopback polarity reversal, as described in section 10.3.1 of [33].
- Not respond to the DSU non-latching loopback codes described in 10.3.2.1 of [33].
- Not respond to the optional DSU latching loopback described in section 10.3.2.2 of [33].

8 ISDN (I.430/I.431)

ITU-T recommendations I.430 and I.431 will be followed. No exceptions to these recommendations are noted in this agreement.

9 T1 (ANSI T1.403/G.703/G.704)

9.1 ANSI T1.403 (1544 Kbps)

ANSI T1.403 [8] will be followed, with the following exceptions:

1) Section 2 - Normative References: The reference to ITU Recommendation Q.921 refers to "ITU, Blue Book Vol. VI - Fascicle VI.10, Recommendation Q.921, Digital Subscriber Signaling System No. 1 (DSS 1), Data Link Layer" [1].
2) Section 6.2.3 - Transmission Rate, Note 3: The older equipment rate variation up to +/- 200 bit/s is not applicable.
3) Section 8.1 - Clear Channel Capability: The text in this section is replaced by the following: To provide DS1 Clear Channel Capability (CCC), a DS1 signal with unconstrained information bits is altered to meet the pulse density requirement of 6.2.9. The method used to provide DS1 CCC is B8ZS. This method shall be used in both directions of transmission.
4) Section 8.3 - Asynchronous Transfer Mode: This section is not applicable.
5) Section 9.4.2 - Message-oriented Signals: Path, test, or idle signal identification messages do not apply.
6) Section 9.4.2.3 - Path- and Test-signal-ID Messages – This section is not applicable.
7) Section 9.4.3 - Special Carrier Applications: Item 3 of the list and note 18 are not applicable.
8) Annex A - Path and Test Signal Identification Message Requirements: This section is not applicable.

9.2 ITU Recommendation G.703

In addition to ANSI T1.403, the sections related to the 1544 kbit/s interface in ITU Recommendation G.703 [11] apply, with the exception of Section 2.5. The text of Section 2.5 is replaced by: `The B8ZS code shall be used because connecting line systems require suitable signal content to guarantee adequate timing information.'

9.3 ITU Recommendation G.704

In addition to ANSI T1.403, the sections related to the 1544 kbit/s interface in ITU Recommendation G.704 [12] apply, with the following exceptions:

1) Section 2.1.3 - Allocation of the F-bit: The current text is to be replaced by: "Table 1/G.704 provides the recommended F-bit allocation."

2) Table 1/G.704 applies as follows:
   a) The column "For character signal is" is modified such that all instances of "1-7" are replaced by "1-8" (related bits are: 966, 2124, 3282 and 4440).
   b) The column "For signalling" is not applicable.
   c) The column "Signalling channel designation" is not applicable.
3) Table 2/G.704: The table is not applicable.
4) Section 2.1.3.1.1 - Multiframe alignment signal: The section starting with "...as well as to identify" to the end of the sentence is not applicable.
5) Section 2.1.3.1.3 - 4 kbit/s data link, third paragraph: The entire paragraph is replaced by: "The idle data link pattern is the HDLC flag bit pattern (01111110)."
6) Section 2.1.3.2 - Method: twelve-frame multiframe: This section is not applicable.
7) Section 3.1.2 - Use of 64 kbit/s channel time slots: This section is not applicable.
8) Section 3.1.3 - Signalling: All sections under 3.1.3 are not applicable.
9) Section 3.2 - Interface at 1544 kbit/s carrying 32 kbit/s channel time slots: All sections under 3.2 are not applicable.
10) Section 3.3 - Interface at 1544 kbit/s carrying n * 64 kbit/s: This section is not applicable.

10 E1 (ITU Recommendation G.703/G.704)

10.1 ITU Recommendation G.703

Applicable sections of the G.703 specification [11] are as follows for support of 2048 Kbps (E1) interfaces:

1) Introduction: Except those references to 1544 Kbps.
2) Section 6: Interface at 2048 Kbps.
3) Annex A: Definition of codes.
4) Annex B: Specification of the overvoltage protection requirement.

10.2 ITU Recommendation G.704

Applicable sections of [12] are as follows:

1) General.
2) Section 2.3: Basic frame structure at 2048 Kbps.
3) Section 5: Characteristics of frame structures carrying channels at various bit rates in 2048 Kbps interfaces where applicable in channelized applications.
4) Annex A.3: CRC-4 procedure for interface at 2048 Kbps.

Note that section 1. General specifies the electrical interface characteristics to be G.703.

11 T3 (ANSI T1.404)

The ANSI T1.404 [28] and T1.404a [29] standards specify the DS3 frame structure for data rates of 44.736 Mbps. Frame relay frames and inter-frame flags are mapped directly into channelized or unchannelized DS3 bit-streams.

All sections of these standards apply with the following exceptions:

1) Section 5.9, Power Level: The alternative power specification of the power of an all ones (1s) signal described in the note.

2) Section 7.2.2.4 – Terminal-to-terminal Path Maintenance Data Link.

3) Section 7.2.2.6 – Terminal-to-terminal Application Specific Data Link.

Further, Section 2, Normative references is modified as follows:

References to ANSI T1.107-1988 and ANSI T1.107a-1990 should reference ANSI T1.107-1995 Section 9.

12 E3 (ITU Recommendation G.703)

ITU Recommendation G.703 [11] includes support for interfaces operating at data rates of 34.368 Mbps. An implementation that supports this G.703 interface rate shall comply with the following sections of [11]:

1) Section 8: Interface at 34.368 Mbps

2) Annex A: Definition of codes

3) Annex B: Specification of the overvoltage protection requirement

ITU Recommendation G.832 [26] describes the framing format. An implementation that supports the G.703 34.368 Mbps interface rate shall also comply with G.832. An implementation that supports the G.703 34.368 Mbps interface rate may optionally support G.751 [27].

13 SONET/SDH (ANSI T1.105/ITU G.707)

Frame Relay uses SONET/SDH transport as full-duplex octet-oriented synchronous links. Bit stuffing is not used; see Section 13.4 for further details. The SONET/SDH interface characteristics documented in RFC 1619 [32] and G.707 (1998) [34] (see Appendix A) form the basis of this agreement to the extent detailed below.

13.1 Interface Format

An octet interface to the physical layer is used. There is no provision for sub-octets to be supplied or accepted.

The octet stream is mapped into the SONET/SDH Synchronous Payload Envelope (SPE), with the octet boundaries aligned with the SPE octet boundaries. HDLC flags (01111110) shall be used for interframe fill to buffer out the asynchronous nature of the arrival of the HDLC framed signals.

Scrambling of HDLC framed signals is required to provide security against emulation of the SDH set-reset scrambler pattern and replication of the STM-N frame alignment word. The $x^{43} + 1$ self-synchronous scrambler is used following byte stuffing (see Section 13.4) during insertion into the SPE. The scrambler shall operate continuously through the bytes of the SPE, including the interframe fill, bypassing bytes of SONET Path Overhead and any fixed stuff (see Figure 20 of ANSI T1.105 [30] or Figure 10-17 of G.707 [31]). The scrambling state at the beginning of a SPE shall be the state at the end of the previous SPE. Thus, the scrambler runs continuously and is not reset per frame. An initial seed is unspecified. Consequently, the first 43 transmitted bits following startup or

reframe operation will not be descrambled correctly. The scrambler operates most significant bit first. The scrambler is fed as follows:

A[7], A[6], … A[0], B[7], B[6], etc…

where A and B are consecutive octets, and A[7] is the most significant bit of octet A. Note that this is the opposite bit order of the HDLC FCS calculation.

The transmitter operation is illustrated in Figure 1.

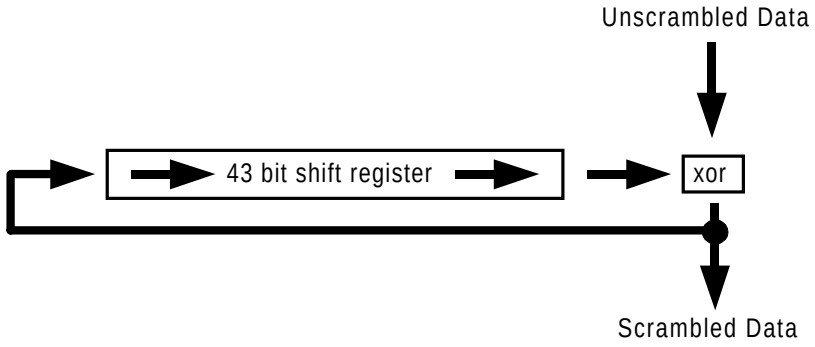

Figure 1
Transmitter Schematic

The receiver operation is illustrated in Figure 2.

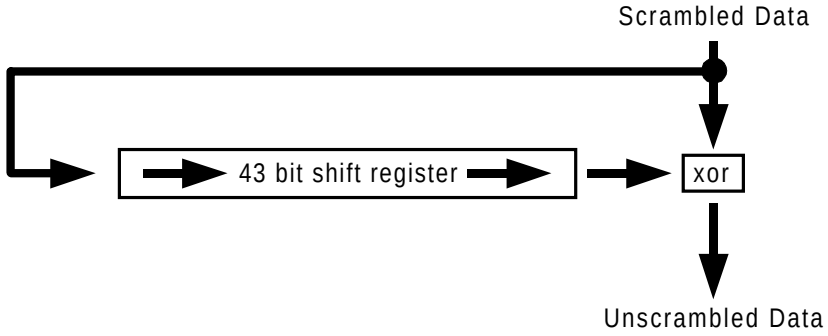

Figure 2
Receiver Schematic

The Path Signal Label (C2) indicates the contents of the SPE. The value of 22 (0x16) is used to indicate a variable-length HDLC frame with scrambling enabled. Implementations must **not** use a Path Signal Label (C2) value of 207 (0xCF), which indicates a variable-length HDLC frame without scrambling.

The Multiframe Indicator (H4) is unused, and must be zero.

13.2 Transmission Rate

The basic rate for Frame Relay over SONET/SDH is that of STS-3c/STM-1 at 155.520 Mbps. The available information bandwidth is 149.760 Mbps, which is the STS-3c/STM-1 SPE with section, line and path overhead removed. This is the same super-rate mapping that is used for ATM and FDDI [30].

Lower signal rates must use the Virtual Tributary (VT) mechanism of SONET/SDH. This maps existing signals up to T3/E3 rates asynchronously into the SPE, or uses available clocks for bit-synchronous and byte-synchronous mapping.

Higher signal rates must conform to the SDH STM series, rather than the SONET STS series. The STM series progresses in powers of 4 (instead of 3), and employs fewer steps, which simplifies multiplexing and integration.

13.3 Control Signals

The use of control signals is not required.

13.4 Framing and Octet Stuffing

Framing and octet stuffing for octet-oriented synchronous links are described in Section 4 of RFC 1662 [13], disregarding sections 4.4.2 and 4.5.2.

FR frames are located by row within the SPE payload. Because frames are variable in length, the frames are allowed to cross SPE boundaries.

13.5 Frame Check Sequence

The 32-bit FCS described in [13] is required to mitigate the error multiplication of this scrambler. The CRC-32 generator polynomial is:

$$G(x) = x32 + x26 + x23 + x22 + x16 + x12 + x11 + x10 + x8 + x7 + x5 + x4 + x2 + x + 1$$

Annex A

This Appendix contains revisions to G.707 (1996), to be included in G.707 (1998), that were approved at the ITU's February 1998 Study Group 15 meeting in Geneva. This appendix will be replaced by a reference to G.707 (1998) after it becomes generally available. This text is excerpted from [34].

12) Signal label (C2) coding.

Action: SG 15
Report: Feb. 98 meeting of SG 15.
Status: Code "16" assigned for mapping of HDLC according to 10.3/G.707 (see item 13).
Code "CF" assigned for mapping of HDLC according to IETF RFC 1619.
Text in ITU-T TIES directory /t2/tSG 15/SG 15/wp3/stable_text/G707/02-98.DOC.

- Modification to paragraph 9.3.1.3 (Signal label: C2)
Modify Table 7/G.707 as follows:

1100	1111	CF (Note 9)	Mapping of HDLC framed signal according to IETF RFC 1619
0001	0110	16	Mapping of HDLC framed signal according to § 10.3/G.707

NOTE 9 - Previous value assigned by IETF for HDLC framed signal, obsoleted by 16

13) Mapping of HDLC framed signals

Action: SG 15
Report: Feb. 98 meeting of SG 15...
Status: New paragraph 10.3 added
Text in ITU-T TIES directory /t2/tSG 15/SG 15/wp3/stable_text/G707/02-98.DOC.

- New paragraph 10.3 (Mapping of HDLC framed signal)
Add the following paragraph:

10.3 Mapping of HDLC framed signals

The mapping of HDLC framed signals according to ISO/IEC 3309 is performed by aligning the byte structure of every frame with the byte structure of the Virtual Container used including the concatenated structure (VC-4-X/VC-4/VC-3). Since the HDLC frames are of variable length (the mapping does not impose any restrictions on the maximum length) a frame may cross the Container-x frame boundary. HDLC flags (01111110) shall be used for interframe fill to buffer out the asynchronous nature of the arrival of the HDLC framed signals according to the effective payload of the Virtual Container used (this excludes any fixed stuff bytes).
The HDLC framed signal plus the interframe fill shall be scrambled before they are inserted as payload of the Virtual Container used. In the reverse operation, following termination of the VC-x or VC-x-mc signal, the payload will be descrambled before it is passed on to the HDLC layer. A self synchronizing scrambler with generator polynomial $x^{43}+1$ shall be used. If a Cyclic Redundancy Check is applied over the HDLC payload signal, a CRC32 is recommended to mitigate the error multiplication of this scrambler. Scrambling of HDLC framed signals is required to provide security against emulation of the SDH set-reset scrambler pattern and replication of the STM-N frame alignment word.

The above mapping procedure shall be used for the mapping of HDLC framed signals in any SDH Virtual Container. There are no specific requirements for any Virtual Container size, other than that the appropriate signal label for that Container is inserted in the appropriate Path Overhead location. Path signal labels are specified in G.707 paragraph 9.3.